In the Claims:

1. (Currently Amended) A memory device capable of controlling a characteristic parameter, comprising:

a register controller for storing control data; and

a parameter controller for receiving an input signal having a characteristic parameter, for controlling the value of the characteristic parameter of the input signal according to the control data and for generating an output signal having the controlled characteristic parameter,

~~a parameter controller configured to output a signal having a characteristic parameter depending on the control data outputted from the register controller,~~ wherein the register controller is nonvolatile.

2. (Currently Amended) The memory device according to claim 1, wherein the register controller comprises:

a register array comprising a plurality of registers for storing the control data; and

a register command processor configured to receive a plurality of signals, to identify a mode ~~as a program mode or a read mode~~ by decoding the plurality of signals, and ~~individually control the plurality of registers to store~~ to read/write the control data from/to the plurality of registers according to the identified mode, wherein the plurality of registers are nonvolatile.

3. (Currently Amended) The memory device according to claim 2, wherein each of the plurality of registers comprises:

a first amplifier configured to amplify and maintain a voltage of a first node having a higher potential between a second node and a third node, at a positive voltage in response to a first control signal;

a second amplifier configured to amplify and maintain a voltage of a fourth node having a lower potential between the second node and the third node, at ground voltage in response to a second control signal;

an input unit configured to provide a data signal to the second node and the third node in response to a third control signal; and

a storage unit configured to store the data signal provided to the second node and the third node in response to a fourth signal, wherein the data signal remains stored while a power is down.

4. (Original) The memory device according to claim 3, wherein the first amplifier comprises:

a first PMOS transistor comprising a gate connected to receive the first control signal and a source connected to a positive power source;

a second PMOS transistor comprising a gate connected to the first node, a source connected to a drain of the first PMOS transistor, and a drain connected to the third node; and

a third PMOS transistor comprising a gate connected to the third node, a source connected to the drain of the first PMOS transistor, and a drain connected to the second node.

5. (Original) The memory device according to claim 3, wherein the second amplifier comprises:

a first NMOS transistor comprising a gate connected to the second node and a drain connected to the third node;

a second NMOS transistor comprising a gate connected to the third node and a drain connected to the second node; and

a third NMOS transistor comprising a gate connected to receive the second control signal, a drain connected to a source of the first NMOS transistor and a source of the second NMOS transistor, and a source connected to ground.

6. (Original) The memory device according to claim 3, wherein the input unit comprises:

a first NMOS transistor comprising a gate connected to receive the third control signal, a source connected to receive a first data signal, and a drain connected to the second node; and

a second NMOS transistor comprising a gate connected to receive the third control signal, a source connected to receive a second data signal, and a drain connected to the third

node.

7. (Original) The memory device according to claim 3, wherein the storage unit comprises:

a first ferroelectric capacitor comprising a first terminal connected to receive the fourth control signal, and a second terminal connected to the second node;

a second ferroelectric capacitor comprising a first terminal connected to receive the fourth control signal, and a second terminal connected to the third node;

a third ferroelectric capacitor comprising a first terminal connected to the second node, and a second terminal connected to ground; and

a fourth ferroelectric capacitor having a first terminal connected to the third node, and a second terminal connected to ground.

8. (Original) The memory device according to claim 2, wherein the register command processor is configured to start a program mode if an output enable signal toggles a predetermined number of times while a write enable signal and a chip enable signal included in the received plurality of signals are activated, and not respond to the write enable signal, the chip enable signal and the output enable signal during the program mode.

9. (Original) The memory device according to claim 1, wherein the memory device is a ferroelectric memory device.

10. (Original) The memory device according to claim 9, wherein the ferroelectric memory device comprises:

a plurality of unit cells;

a plurality of switches; and

bitlines comprising sub bitlines connected to the plurality of unit cells and a main bitline connected to the plurality of sub bitlines via the plurality of switches,

wherein the plurality of switches is configured so that when a predetermined unit cell of

the plurality of unit cells is accessed, only a switch for connecting a particular one of the plurality of sub bitlines connecting the predetermined unit cell to the main bitline is turned on, and other switches for connecting the rest of the plurality of sub bitlines to the main bitline are all turned off.

Claims 11-18 (Withdrawn).

Claim 19 (Canceled).

20. (Currently Amended) An integrated circuit device ~~according to claim 19, wherein the signal performance characteristic controller~~ capable of controlling signal performance characteristics of an input signal to generate an output signal having the controlled signal performance characteristics, ~~comprises~~ comprising:

a register controller configured to provide a plurality of control signals;

a plurality of nonvolatile registers each coupled to the register controller to receive one of the plurality of control signals and for storing and outputting a control data signal; and

a plurality of transistors each comprising a source coupled to a voltage ~~source,~~ source and a gate configured to receive the control data signal from ~~at least~~ one of the plurality of nonvolatile registers, ~~and a drain,~~ wherein ~~each of the~~ drains of the plurality of transistors are coupled to provide a common ~~output,~~ output which is used to control the signal performance characteristics.

~~wherein the common output controls the signal performance characteristic of the output signal from the integrated circuit device.~~